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10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Computer Communication Network

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With layer diagram, explain the responsibility of each layer in OSI model. **(09 Marks)**

b. Explain the operation of ADSL using discrete multitone modulation with a neat diagram. **(06 Marks)**

c. List different types of addressing in TCP. Explain any one type of addressing with a suitable example. **(05 Marks)**

2 a. Distinguish character stuffing and bit stuffing, with an example. **(04 Marks)**

b. Explain different HDLC frames. **(06 Marks)**

c. What are sliding window protocols? Design Go-Back-N ARQ protocol for noisy channel. **(10 Marks)**

3 a. Explain non persistant, *l*-persistent and p-persistent with flow diagram. **(06 Marks)**

b. Explain Token passing as a controlled access technique. **(04 Marks)**

c. With a suitable example, explain data communication on a CDMA/CD network. Also list the properties of chip Sequences. **(10 Marks)**

4 a. Explain addressing mechanism used in IEEE 802.11. **(06 Marks)**

b. Explain the standard Ethernet physical layer implementation of, (i) 10 base 2 (ii) 10 base 5 (iii) Twisted pair Ethernet (iv) Fibre Ethernet. **(08 Marks)**

c. Explain the IEEE 802.3 MAC frame format of standard Ethernet. **(06 Marks)**

PART – B

5 a. Explain spanning tree algorithm with graphical representation. **(06 Marks)**

b. Explain the characteristics of VLAN used to group stations and explain them briefly. **(06 Marks)**

c. Explain the following interconnecting devices:
(i) Repeater (ii) Bridges (iii) Router (iv) Gateway **(08 Marks)**

6 a. Compare between IPV4 and IPV6 extension headers. **(06 Marks)**

b. Describe three strategies devised by IETF to help transition from IPV4 to IPV6. **(06 Marks)**

c. An ISP is granted a block of address strating with 190.100.0.0/16 the ISP needs to distribute these addresses to three group of customers as follows:
i) The first group has 64 customers, each need 256 addresses.
ii) The second group has 128 customers, each need 128 addresses.
iii) The third group has 128 customers, each need 64 addresses.
Design sub blocks and find out how many addresses are still available after these allocations. **(08 Marks)**

7 a. Write short notes on :
   i) Forwarding process.
   ii) Address aggregation.
   iii) Dynamic routing table. **(15 Marks)**

   b. What are the basis for classification of four types of links defined by OSPF? **(05 Marks)**

8 a. With a neat diagram, explain briefly connection establishment, date transfer, connection termination and half close connection in TCP. **(12 Marks)**

   b. With regards to DNS in internet,
   i) Explain briefly recursive and iterative resolution.
   ii) Query and response messages. **(08 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Optical Fiber Communications

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What are the advantages and disadvantage of optical fiber communication? **(07 Marks)**

b. Derive necessary mathematical condition that the angle of incidence "θ" must satisfy for the optical skew ray to propagate in a step index fiber. **(08 Marks)**

c. Calculate the number of modes of an optical fiber having diameter of 50 μm, $n_1 = 1.48$, $n_2 = 1.46$ and wavelength 'λ' of 820 nm. **(05 Marks)**

2 a. Explain the different types of absorption losses in optical fiber. **(06 Marks)**

b. Derive an expression for pulse spreading due to material dispersion which is a function of wavelength and time delay. **(08 Marks)**

c. Explain the different types of bending losses in optical fiber. **(06 Marks)**

3 a. Draw the cross section of GaALAS double hetero structure LED energy band diagram and refractive index variation. Explain their importance. **(07 Marks)**

b. Derive an expression for lasing condition and hence for optical gain in LASERS. **(08 Marks)**

c. With proper sketch briefly explain the structure of RPAD photodiode. **(05 Marks)**

4 a. Show that optical power coupled into a step index fiber due to an LED with lambartian distribution is given by $P = P_S(NA)^2$ for $r_S \leq a$, with usual notations. **(07 Marks)**

b. What are different types of mechanical misalignments? **(05 Marks)**

c. Explain briefly the various fiber splicing techniques. **(08 Marks)**

PART – B

5 a. With neat diagram, explain the operation of transimpedance preamplifier equivalent circuit. **(06 Marks)**

b. Derive an expression for receiver sensitivity and also explain quantum limit. **(08 Marks)**

c. Discuss how the eye diagram is powerful measurement tool for assessing the data handling capability in digital transmission system. **(06 Marks)**

6 a. Explain with block diagram, the elements of analog link. List the signal impairments in analog systems. **(06 Marks)**

b. Explain sub-carrier multiplexing techniques in optical fiber communication. **(04 Marks)**

c. Briefly explain the rise time budget analysis with its basic elements contribute to system risetime. **(10 Marks)**

7 a. With a neat sketch, explain WDM scheme. **(05 Marks)**

b. Derive an expression for difference in length in MZI multiplexers. **(09 Marks)**

c. Write a note on optical add | drop multiplexers. **(06 Marks)**

8 a. Explain in detail the amplification mechanism with energy level diagram in an EDFA. **(10 Marks)**

b. With suitable diagram describe SONET/SDH optical network function. **(10 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain five types of power electronic converter circuits briefly. Also indicate two applications of each type. **(10 Marks)**

b. What are the peripheral effects of power electronics equipments? **(06 Marks)**

c. Give symbol, and characteristic features of the following devices: i) GTO; ii) TRIAC. **(04 Marks)**

2 a. What is the necessity of base drive control in a power transistor? Explain proportional base control. **(08 Marks)**

b. The bipolar transistor of Fig.Q.2(b) is specified to have β in the range 8 to 40. The load resistance is $R_C = 11\Omega$. The dc supply voltage is $V_{CC} = 200V$ and the input voltage to the base circuit is $V_B = 10V$, $V_{CE(sat)} = 1V$ and $V_{BE(sat)} = 1.5V$. Find:

i) The value of R_B that results in saturation with an overdrive factor of 5.

ii) The forced β_f.

iii) The power loss P_T in the transistor. **(08 Marks)**

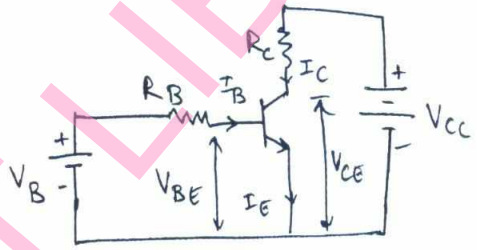

Fig.Q.2(b)

c. Give the comparison between MOSFET and IGBT. **(04 Marks)**

3 a. Draw the two transistor model of a thyristor and derive an expression for the anode current interms of the common base current gain α_1 and α_2 of the transistors. **(10 Marks)**

b. An UJT is used to trigger the thyristor whose minimum gate trigging voltage is 6.2V. The UJT ratings are: $\eta = 0.66$, $I_P = 0.5mA$, $I_V = 3mA$, $R_{B1} + R_{B2} = 5k\Omega$, leakage current = 3.2mA, $V_P = 14V$ and $V_V = 1V$. Oscillator frequency is 2kHz and capacitor $C = 0.04\mu F$. Design the complete circuit. **(10 Marks)**

4 a. With a neat circuit diagram and waveforms, explain the working of a single phase full converter feeding highly inductive load. Derive the expression for the average output voltage and rms output voltage. **(10 Marks)**

b. With a neat circuit diagram and waveforms, explain the principle of operation of dual converter with circulating current. **(04 Marks)**

c. What are the advantages and drawbacks of circulating current mode of operation of a dual converter? **(06 Marks)**

PART – B

5 a. Explain the working of step down choppers with waveforms and derive the equation for output voltage. **(06 Marks)**

b. Explain the working of boost regulator and derive the expression for average output voltage. **(06 Marks)**

c. A buck regulator has an input voltage of 12V. The required average output voltage is 5V at R = 5Ω and peak-to-peak output ripple voltage is 20mV. The switching frequency is 25kHz. If the peak-to-peak ripple current of inductor is limited to 0.8A, determine: i) duty cycle; ii) filter inductance L; iii) Filter capacitance; iv) Critical values of L and C. **(08 Marks)**

6 a. What do you mean by commutation? With necessary circuit and waveforms, explain self commutation scheme. **(10 Marks)**

b. With a neat circuit diagram and waveforms, explain the auxiliary commutation (impulse commutation). **(10 Marks)**

7 a. Explain the working of ON/OFF controllers and derive an expression for output rms voltage. **(06 Marks)**

b. An ACVC is provided with a load of 10Ω, supplied with an AC voltage of 120V, 50Hz with 25 cycles ON and 75 cycles OFF. Calculate the power dissipated in the resistance, rms current in each of the SCR's and average current in each of the SCR's. **(06 Marks)**

c. A single phase full wave AC controller has a load resistance of R = 10Ω and input voltage of 120V, 60Hz. The delay angle for both the thyristors is π/2. Determine rms value of output voltage, input power factor and average thyristor current. **(08 Marks)**

8 a. Explain single phase half bridge inverter with R-load with necessary circuit diagram and waveforms. Derive the equation for rms output voltage. **(08 Marks)**

b. Explain the performance parameters of inverters. **(08 Marks)**

c. Give the comparison between voltage source inverter and current source inverter. **(04 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain a microprocessor based embedded system with diagram. **(08 Marks)**

b. With necessary block diagram, explain the embedded system life cycle. **(08 Marks)**

c. Explain the important steps in developing a embedded system. **(04 Marks)**

2 a. Analyze how errors propogate under : (i) Addition process (ii) Multiplication process. **(08 Marks)**

b. With the help of diagram, explain
(i) Index mode data transfer operation.
(ii) Program counter relative operation. **(08 Marks)**

c. With timing diagram, explain (i) Writing to a register (ii) Reading from a register. **(04 Marks)**

3 a. With diagram, explain direct mapping implementation and associative mapping cache implementation. **(08 Marks)**

b. With diagram, explain the operation of DRAM. With timing diagram, explain read operation. **(08 Marks)**

c. Explain the concept of dynamic memory allocation. **(04 Marks)**

4 a. Develop hardware and software specification for designing a counter and give data control flow diagram. **(08 Marks)**

b. With diagram explain (i) Water fall life cycle model (ii) Spiral life cycle model. **(08 Marks)**

c. Compare functional model and architectural model. **(04 Marks)**

PART – B

5 a. Explain how memory is managed at,
(i) System level (ii) Process level. **(08 Marks)**

b. Explain operating system architecture with diagram. **(08 Marks)**

c. Explain multithreaded OS. **(04 Marks)**

6 a. Organize general purpose registers as,
(i) Four different contexts (ii) Overlapping contexts. **(08 Marks)**

b. Explain the structure of TCB with diagram. **(08 Marks)**

c. With diagram, explain real time stack and application stack. **(04 Marks)**

7 a. Analyze the basic flow of control construct in, (i) Constant time statements (ii) Sequence of statements (iii) For loops (iv) While loops. **(08 Marks)**

b. Explain the 3 methods used to compute time loading. **(08 Marks)**

c. What is a co-routine? Explain. **(04 Marks)**

8 a. Explain a typical memory map with diagram and explain the design of memory map with reference to memory loading. **(08 Marks)**

b. Explain caches and their performance. **(08 Marks)**

c. Write explanatory note on hardware accelerators. **(04 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT x(k), determine analog and digital frequency spacing between adjacent x(k) elements. Also, determine analog and digital frequencies corresponding to k = 64. **(06 Marks)**

b. With a neat block diagram, explain scheme of a DSP system. **(08 Marks)**

c. Let x[n] = [3, 2, -2, 0, 7]. It is interpolated using an interpolation filter b_k = [0.5, 1, 0.5] with interpolation factor 2. Determine the interpolated sequence. **(06 Marks)**

2 a. With a neat block diagram, explain arithmetic logic unit (ALU) of a DSP system. **(06 Marks)**

b. Explain the operation of barrel shifter, with an example. **(05 Marks)**

c. Explain : i) circular addressing mode ii) parallelism iii) Guard bits. **(09 Marks)**

3 a. Explain functional architecture of TMS320C54XX processor, with a block diagram. **(10 Marks)**

b. Explain the addressing modes of TMS320C54XX processor. Give examples. **(10 Marks)**

4 a. Explain the following assembler directives of TMS320C54XX processors.
i) · mmregs ii) · global iii) · include'xx' iv) · data v) · end vi) · bss **(06 Marks)**

b. Describe Host port interface and explain its signals. **(06 Marks)**

c. Write an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation, $y(n) = h_0\, x(n) + h_1\, x(n-1) + h_2\, x(n-2)$ with usual notations. Find y(n) for signed 16 bit data samples and16 bit constants. **(08 Marks)**

PART – B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a Q0 number ii) 4400h as a Q7 number iii) ·3125 as a Q15 number iv) –·3125 as a Q15 number. **(06 Marks)**

b. Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result. **(06 Marks)**

c. What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and polyphase subfilter. **(08 Marks)**

6 a. Write a TMS320C54XX program that illustrates the implementation of 8-point DIT FFT algorithm. **(12 Marks)**

b. Briefly explain scaling and derive the expression for optimum scaling factor for DIT FFT Butterfly algorithm. **(08 Marks)**

7 a. With a neat schematic diagram, design a data memory system with address range 000800h – 000FFFH for a C5416 processor. Use 2K×8 SRAM memory chips. **(08 Marks)**

b. Explain how the interrupts are handled in TMS320C54XX processor, with the help of a flow chart. **(08 Marks)**

c. Explain briefly memory space organization in TMS320C54XX memory. **(04 Marks)**

8 a. Explain PCM3002 CODEC, with the help of a neat block diagram. **(06 Marks)**

b. Explain DSP-based biotelemetry receiver system, with the help of a block schematic diagram. **(06 Marks)**

c. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(08 Marks)**

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10EC762

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Real Time System

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define real time system. Classify them based on time constraints. **(04 Marks)**

b. Explain the different types of programs in system design. **(06 Marks)**

c. Explain in detail, the generalized computer control system showing hardware and software interface. **(10 Marks)**

2 a. List out the activities and objectives carried out by computer in computer control application. **(06 Marks)**

b. What is DDC? Explain in brief the different possible techniques used for it. **(10 Marks)**

c. Write a note on hierarchical system. **(04 Marks)**

3 a. What is necessity of using specialized processors in RTS? Explain the different forms of parallel computer architectures. **(10 Marks)**

b. Explain the basic interrupt input mechanism with diagram and flow chart. **(06 Marks)**

c. Explain multilevel interrupts. **(04 Marks)**

4 a. List and explain in brief, the major requirement for a real time language. **(12 Marks)**

b. Explain with block diagram, the table driven approach to devise special application software. **(08 Marks)**

PART – B

5 a. Explain with neat diagram, the typical structure of a RTOS. **(06 Marks)**

b. List the basic functions of the task management. Explain the task states with the help of task state diagram. **(08 Marks)**

c. Explain the three levels of priority structure. **(06 Marks)**

6 a. Describe in brief mutual exclusion. **(04 Marks)**

b. Explain the general structure of input output sub system (IOSS). **(06 Marks)**

c. Explain the issues of synchronization and communication in inter task communication. **(10 Marks)**

7 a. With respect to real time design, describe the single program approach with flow chart. **(08 Marks)**

b. Explain with diagram, how data will be shared with common memory. **(06 Marks)**

c. With diagram, describe basic software module. **(06 Marks)**

8 a. Explain in detail Hartley and Pirbhai method. **(10 Marks)**

b. Explain with respect to Ward and Mellor method, the following:
   i) Dry-oven context diagram.
   ii) First level transformation diagram for dry-oven. **(10 Marks)**

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